ANALOG DEVICES

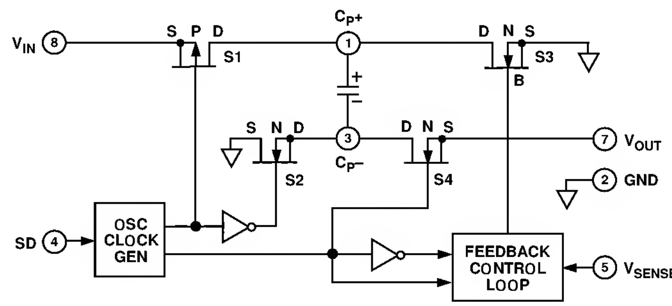
Switched Capacitor Voltage Converter with Regulated Output

ADP3603*

FEATURES
Fully Regulated Output
High Output Current: 50 mA
120 mA Version (ADP3604) Is Also Available
Outstanding Precision: ±3% Output Accuracy
Input Voltage Range: +4.5 V to +6.0 V
Output Voltage: –3.0 V (Regulated)
High Switching Frequency: 120 kHz (240 kHz Internal Oscillator)
Shutdown Capability
Small Outline 8-Pin SOIC Package

APPLICATIONS
Voltage Inverters
Negative Voltage Regulators
Computer Peripherals and Add-On Cards
Portable Instruments
Battery Powered Devices
Pagers and Radio Control Receivers
Disk Drives
Mobile Phones

FUNCTIONAL BLOCK DIAGRAM

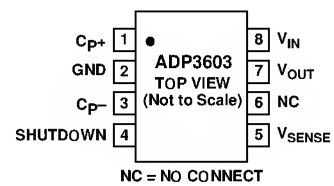


GENERAL DESCRIPTION
The ADP3603 switched capacitor voltage converter provides a regulated output voltage with minimum voltage loss and requires a minimum number of external components. In addition, the ADP3603 does not require the use of an inductor. The ADP3603 provides up to 50 mA of output current with ±3% output accuracy.

The internal oscillator runs at 240 kHz nominal frequency which produces an output switching frequency of 120 kHz, allowing the use of small charge pump and filter capacitors. The ADP3603 is primarily designed for use as a high frequency negative voltage regulator/inverter. The output voltages of the ADP3603 can range from –1.2 V to –4.0 V, nominally –3.0 V. For other output voltages, contact the factory.

The ADP3603 dissipates less than 150 mW of power and features fast shutdown mode capability (<5 ms) that also drops the quiescent current to 1.4 mA (typ). For a higher output current (120 mA) version, see the ADP3604.

PIN CONFIGURATION
8-Pin SOIC
(SO-8)



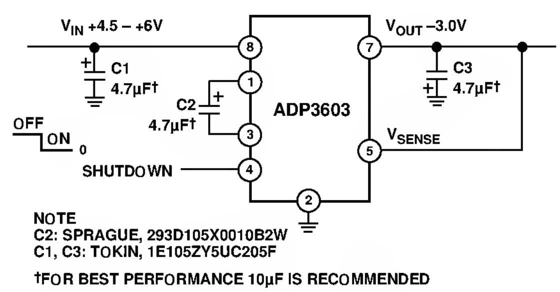


Figure 1. Typical Application Circuit

*Patent pending.

REV. 0

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ADP3603–SPECIFICATIONS (V_{IN} = 5.0 V @ T_A = +25°C, C_P = C_{OUT} = 10 µF unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
OPERATING SUPPLY RANGE	V_S		4.5	5	6	V
SUPPLY CURRENT	I_S			2.4	3	mA
		–40°C < T_A < +85°C		2.5	3.5	mA
Shutdown Mode				1.4	2	mA
		–40°C < T_A < +85°C		1.5	2.5	mA
OUTPUT						
Output Voltage	V_O	I_O = 25 mA	–3.1	–3	–2.91	V
	V_O	I_O = 10 mA to 50 mA, 4.5 V < V_{IN} < 6 V	–3.1	–3	–2.9	V
	V_O	I_O = 10 mA to 50 mA, 4.5 V < V_{IN} < 6 V, 0°C < T_A < +70°C	–3.12	–3	–2.88	V
	V_O	I_O = 10 mA to 50 mA, 4.5 V < V_{IN} < 6 V, –40°C < T_A < +85°C	–3.15	–3	–2.85	V
Load Regulation	$\Delta V_O/I_O$	I_O = 10 mA–60 mA		0.9		mV/mA
		I_O = 10 mA–120 mA		1.5		mV/mA
Output Resistance[2]	R_O			8		Ω
Output Ripple Voltage[3]	V_{RIPPLE}	C1–C3 = 10 µF, I_{LOAD} = 80 mA		25		mV
		I_{LOAD} = 120 mA		55		mV
SWITCHING FREQUENCY	F_S		100	120	130	kHz
		–40°C < T_A < +85°C	96	120	140	kHz
SHUTDOWN						
Logic Input High	V_{IH}		2.4			V
Input Current	I_{IH}			1		µA
Logic Input Low	V_{IL}				0.4	V
Input Current	I_{IL}			1		µA
Turn-On-Time	t_{ON}	Figure 1, I_L = 120 mA		5		ms
Turn-Off-Time	t_{OFF}	Figure 1, I_L = 120 mA		5		ms

NOTES
[1]Capacitors C1 and C2 used in the test circuit are 10 µF with 0.1 Ω ESR. Capacitors with higher ESR may reduce output voltage and efficiency.
[2]Open-loop output resistance.
[3]See Figure 1 conditions.

All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

Input Voltage (V+ to GND, GND to OUT) . . . . +7.5 V
Output Short Circuit Protection .1 sec
Power Dissipation, SO-8 . . . . .660 mW
  θ_{JA}[2] . . . . 150°C/W
  θ_{JC} . . . . 41°C/W
Operating Temperature Range . . . .–40°C to +85°C
Storage Temperature Range . . . .–65°C to +150°C
Lead Temperature Range (Soldering 10 sec) . . . . +300°C
  Vapor Phase (60 sec) . . . . +215°C
  Infrared (15 sec) . . . . +220°C

NOTES
[1]This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]θ_{JA} is specified for worst case conditions with device soldered on a circuit board.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADP3603AR	–40°C to +85°C	SO-8

*SO = Small Outline Package.

PIN DESCRIPTION

Pin	Function
1	C_P+, Pump Capacitor Positive Input.
2	Ground.
3	C_P–, Pump Capacitor Negative Input.
4	Shutdown, Logic Level Shutdown Pin. Application of a logic low to this pin will place the regulator in normal operation. The device will be put into shutdown mode with the shutdown pin pulled to V_{IN}. In Shutdown mode the charge pump is turned off. Connect to ground for normal operation.
5	V_{SENSE}, Output Voltage Sense Line. This is used to improve load regulation performance by eliminating IR drop on the output traces. See application section for more detail. For normal operation, connect Pin 5 to V_{OUT} (Pin 7).
6	NC, No Internal Electrical Connection.
7	V_{OUT}, Output Pin. Regulated negative output voltage. Connect a low ESR capacitor between this pin and device GND.
8	V_{IN}, Positive Supply Input when 4.5 V ≤ V_{IN} ≤ 6 V. Connect a low-ESR bypass capacitor between this pin and the device ground pin.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3603 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

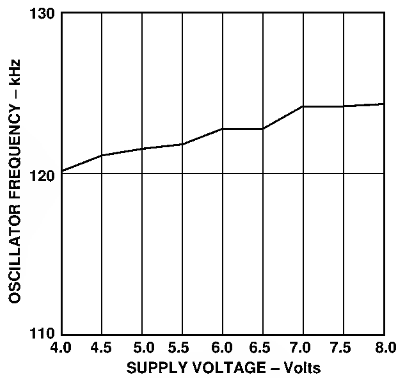


Figure 2. Oscillator Frequency vs. Supply Voltage

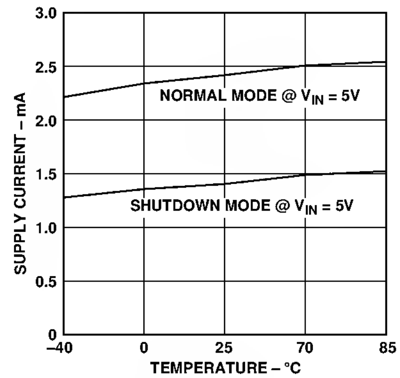


Figure 3. Supply Current vs. Temperature

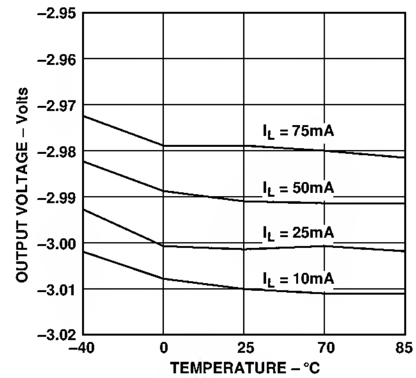


Figure 4. Output Voltage vs. Temperature

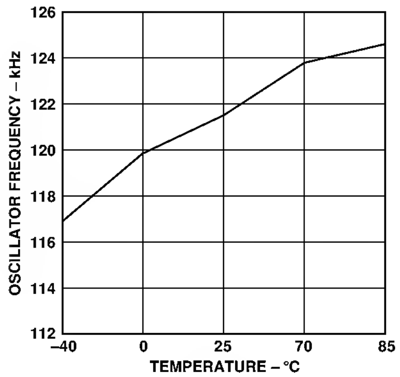


Figure 5. Oscillator Frequency vs. Temperature

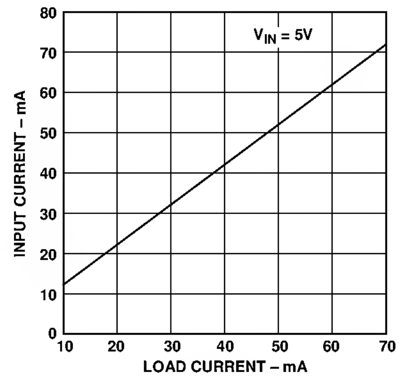


Figure 6. Average Input Current vs. Load Current

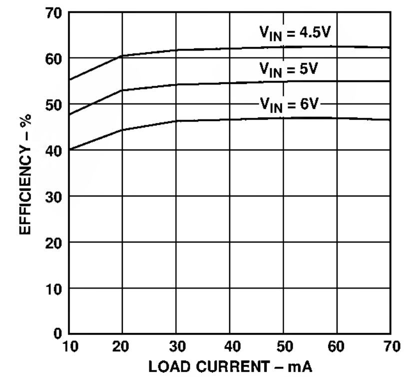


Figure 7. Efficiency vs. Load Current and Input Voltage

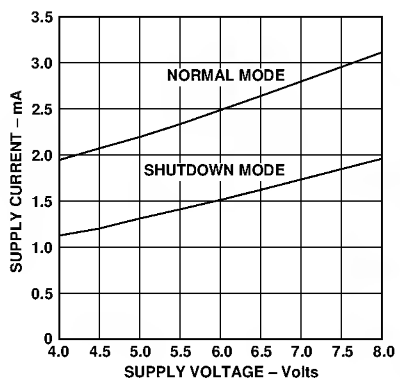


Figure 8. Supply Current vs. Supply Voltage

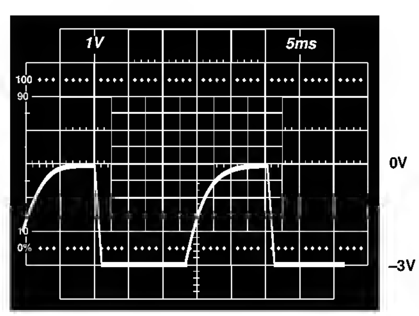


Figure 9. Start-Up Under Full Load

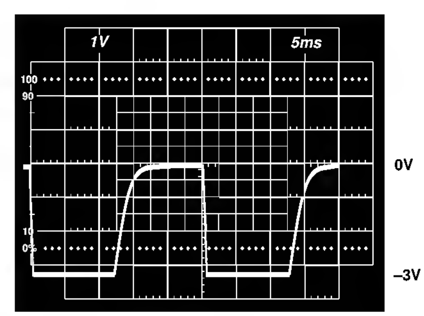


Figure 10. Enable/Disable Time Under Full Load

APPLICATION INFORMATION

The ADP3603 uses a charge pump to generate a negative output voltage from a positive input supply. To understand the operation of the ADP3603, a review of a basic switch capacitor building block is helpful.

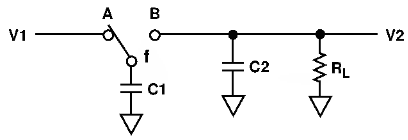


Figure 11. Basic Switch Capacitor Circuit

In Figure 11, when the switch is in the A position, capacitor C1 will be charged to voltage V1. The total charge on C1 will be q1 = C1V1.

The switch then moves to the B position, discharging C1 to voltage V2. After this discharge time, the charge on C1 is q2 = C1V2. The amount of charge transferred from the source, V1, to the output, V2, is:

$$\Delta q = q1 - q2 = C1\,(V1 - V2)$$

If the switch is cycled f times per second, the charge transfer per unit time (i.e., current) is:

$$I = f\,\Delta q = f\,C1\,(V1 - V2)$$

To obtain an equivalent resistance for the switched-capacitor network we can rewrite this equation in terms of voltage and impedance equivalence:

$$I = (V1 - V2)/(1/fC1) = (V1 - V2)/R_{EQUIV}$$

where R_{EQUIV} is defined as:

$$R_{EQUIV} = 1/f\,C1$$

Figure 11 equivalent circuit can now be drawn as shown in Figure 12.

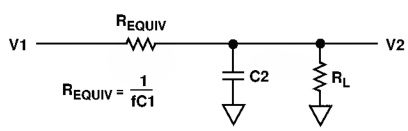


Figure 12. Basic Switch Capacitor Equivalent Circuit

THEORY OF OPERATION

A switched capacitor principle is used in the ADP3603 to generate a negative voltage from a positive input voltage. An on-board oscillator generates two phase clocks to control a switching network which transfers charge between the storage capacitors. The basic principle behind the voltage inversion scheme is illustrated in Figures 13 and 14.

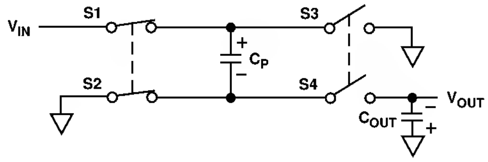


Figure 13. ADP3603 Switch Configuration Charging the Pump Capacitor

During phase one, S1 and S2 are ON charging the pump capacitor to the input voltage. Before the next phase begins, S1 and S2 are turned OFF as well as S3 and S4 to prevent any overlap. S3 and S4 are turned ON during the second phase (see Figure 14) and charge stored in the pump capacitor is transferred to the output capacitor.

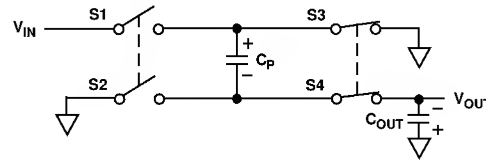


Figure 14. ADP3603 Switch Configuration Charging the Output Capacitor

During the second phase, the positive terminal of the pump capacitor is connected to ground and the negative terminal is connected to the output, resulting in a voltage inversion at the output terminal. Output regulation is done by adjusting the ON resistance of the S3 through the feedback control loop.

The ADP3603 alternately charges C_P to the input voltage when C_P is switched in parallel with the input supply, and then transfers charge to C_{OUT} when C_P is switched in parallel with C_{OUT}. Switching occurs at 120 kHz rate. During the time that C_P is charging, the peak current is approximately 2 times the output current. During the time that C_P is delivering charge to C_{OUT}, the supply current drops down to about 2 mA. An input supply bypass capacitor will supply part of the peak input current drawn by the ADP3603, and average out the current drawn from the supply. A minimum input supply bypass capacitor of 1 µF, preferably a low ESR capacitor such as tantalum or multilayer ceramic chip capacitor, is recommended. A large capacitor may be desirable in some cases, for example when the input supply is connected to the ADP3603 through long leads, or when the pulse current drawn by the device might effect other circuitry through supply coupling.

The output capacitor, C_{OUT}, is alternately charged to the C_P voltage when C_P is switched in parallel with C_{OUT}. The ESR of the C_{OUT} introduces steps in the V_{OUT} waveform whenever the charge pump charges C_{OUT}. This tends to increase V_{OUT} ripple. Ceramic or tantalum capacitors are recommended for C_{OUT} if minimum ripple is desired. The ADP3603 can operate with a range of capacitors from 1 µF to 100 µF and larger without any stability problems. However, all tested parameters are obtained using 10 µF multilayer ceramic capacitors.

In most applications, IR drops due to printed circuit board traces do not present a problem. In this case, V_{SENSE} is tied to the output at a convenient pcb location not far from the V_{OUT}. However, if a reduction in IR drops or improvement in load regulation is desired, the sense line can be used to monitor the output voltage at the load. To avoid excessive noise pickup, the V_{SENSE} line should be as short as possible and away from any noisy line.

Capacitor Selection

While the exact values of the C_{IN} and C_{OUT} are not critical, good quality, low ESR capacitors such as solid tantalum and multilayer ceramic capacitors are recommended to minimize voltage losses at high currents. For a given load current, factors affecting the output voltage performance are in Figure 15:

- Pump (C2) and the output (C3) capacitance
- ESR of the C2 and C3.

Since output current is supplied solely by the output capacitor C3 during one-half of the charge-pump cycle, peak-to-peak output ripple voltage is calculated by using the following formula:

$$V_{RIPPLE} = \frac{I_{OUT}}{2(F_{PUMP})(C2)} + I_{OUT}(ESR_{C2})$$

In Figure 15, output ripple voltage vs. capacitance and various ESR are shown.

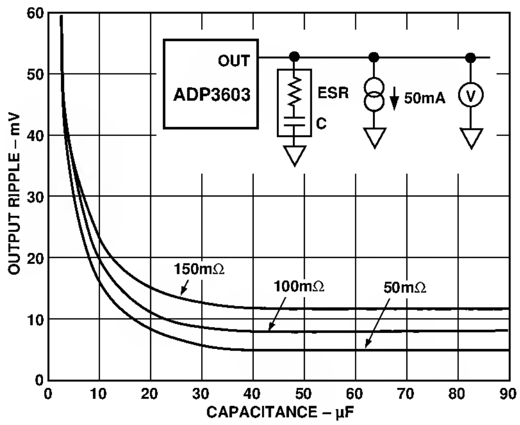


Figure 15. Output Ripple Voltage (mV) vs. Capacitance and ESR

Note that as the capacitor value increases beyond the point where the dominant contribution to the output ripple is due to the ESR, no significant reduction in V_{OUT} ripple is achieved by added capacitance.

A low ESR capacitor has much greater impact on performance for C2 than C3 since current through C2 is twice the C3 current. There is a voltage drop across C_P's ESR during the charge as well as during discharges. Therefore, the voltage drop due to C2 is about 4 times C2's ESR times the load current. The voltage drop generated by C2's ESR combined with the voltage drop due to the output source resistance, determines the maximum available V_{OUT}, while C3's ESR affects the output voltage ripple.

When selecting the capacitors, keep in mind that not all manufacturers guarantee capacitor ESR in the range required by the circuit. In general, the capacitor's ESR is inversely proportional to its physical size, so larger capacitance values and higher voltage ratings tend to reduce ESR.

ESR is also a function of the operating frequency. When selecting a capacitor, make sure its value is rated at the circuit's operating frequency. The other factor affecting the capacitor's performance is temperature. If the circuit has to operate at temperatures significantly different than 25°C, the capacitance and ESR values must be carefully selected to adequately compensate for the change. Various capacitor technologies offer improved performance over temperature, for example, certain tantalum capacitors provide good low-temperature ESR but at a higher cost.

Figure 16 demonstrates the effect temperature has on various capacitors. ADP3603's high internal oscillator frequency permits the usage of smaller capacitance for both the pump and the output capacitors.

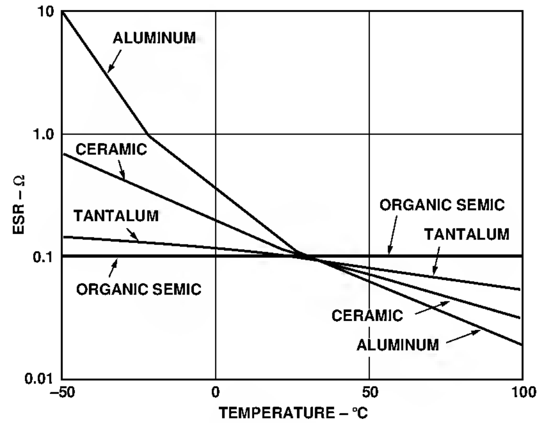


Figure 16. ESR vs. Temperature

Table I. Alternative Capacitor Technologies

Type	Life	High Frequency	Temp	Size	Cost
Aluminum Electrolytic Capacitor	Fair	Fair	Fair	Small	Low
Multilayer Ceramic Capacitor	Long	Good	Poor	Fair	High
Solid Tantalum Capacitor	Above Avg	Avg	Avg	Avg	Avg
OS-CON Capacitor	Above Avg	Good	Good	Good	Avg

Table II shows a partial list of manufacturers providing low-ESR capacitors.

Table II. Recommended Capacitor Manufacturers

Manufacturer	Capacitor	Capacitor Type
Sprague	672D, 673D, 674D, 678D	Aluminum Electrolytic
Sprague	675D, 173D, 199D	Tantalum
Nichicon	PF & PL	Aluminum Electrolytic
Mallory	TDC & TDL	Tantalum
TOKIN	MLCC	Multilayer Ceramic
muRata	GRM	Multilayer Ceramic

EXTERNAL OUTPUT FILTERING

In applications requiring very low power supply ripple and noise, the circuit in Figure 17 provides low noise and ripple of less than 2% of the output voltage over the full load current and temperature.

The output current is supplied solely by the output capacitor C3 during one-half of the charge-pump cycle. This introduces a peak-to-peak ripple of:

$$V_{RIPPLE} = \frac{I_L}{2 \times 120\ kHz \times C3} + I_L \times ESR_{C3}$$

For a nominal F pump of 120 kHz (one-half the nominal 240 kHz oscillator frequency) and C3 = 10 µF with an ESR of 0.15 Ω, ripple voltage is approximately 30 mV with a 50 mA load current.

Multilayer Ceramic Capacitors (MLCC) offer great performance and small size. Using multiple capacitors connected in parallel yields lower ESR and a potential saving in cost. Lighter loads require proportionally smaller capacitors. To reduce high frequency noise, bypass the output with a 0.1 µF ceramic capacitor.

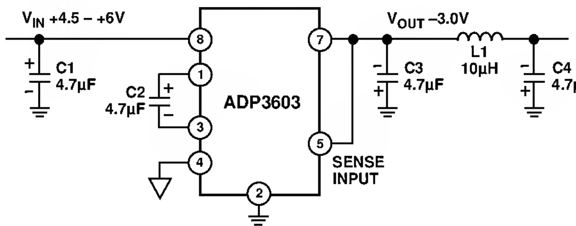


Figure 17. Circuit with Improved Output Ripple & Noise Voltage

Table III. Recommended Components for Circuit in Figure 17

Component	Manufacturer/Type
C2	Sprague, 293D475X0035D2W
C1, C3, C4	TOKIN, 1E475ZY5U-C205-F
L1	Coiltronics, CTX32CT

EXTERNAL INPUT FILTERING

If the ADP3603 is supplied from a high-impedance source, connect an additional bypass capacitor from V+ to ground. Low-ESR capacitors of up to 100 µF give best results. Place external capacitors close to the supply pins of the device with the ground connection made as close to the device ground as possible. The same ground point should be used for the output bypass capacitor.

Smaller bypass capacitors can be used in conjunction with a π-LC filter.

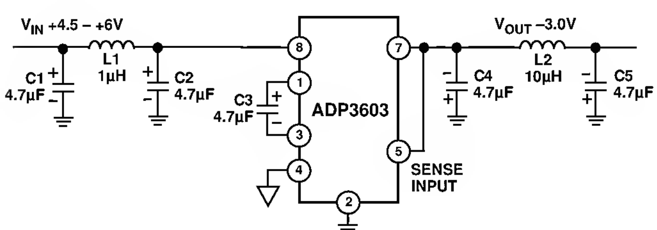


Figure 18. Circuit with Reduced Input and Output Ripple & Noise Voltage

Table IV. Recommended Components for Circuit in Figure 18

Component	Manufacturer/Type
C3	Sprague, 293D475X0035D2W
C1, C2, C4, C5	TOKIN, 1E475ZY5UC205F
L1	Coiltronics, CTX32CT-1R0
L2	Coiltronics, CTX32CT-100

SHUTDOWN MODE

ADP3603's output can be turned off by utilizing the shutdown pin, Pin 4. Pulling the shutdown pin high to a TTL/CMOS logic compatible level will stop the internal oscillator and turn OFF the output pass transistor. A digital low level will turn the output ON. If the shutdown feature of the device is not used, Pin 4 should be tied to the ground pin of the device.

MAXIMUM OUTPUT VOLTAGE

Maximum unregulated output voltage can be obtained by connecting the sense pin to ground instead of the V_{OUT} pin as shown in Figure 19.

Under this condition, the magnitude of the unregulated output voltage depends on the load current. V_{OUT} is inversely proportional to the load current as shown on the graph in Figure 19.

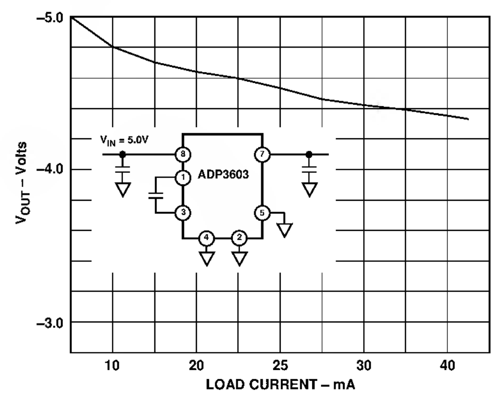


Figure 19. Maximum Unregulated Output Voltage

Under light loads, 30 mA < I_{LOAD}, a regulated output voltage between –3.0 V to $-V_{IN}$ V is possible by inserting a resistor between the sense pin and the V_{OUT} pin as shown in Figure 20. The output voltage is approximated using the following formula:

$$V_{OUT} = -(3 + R/5)$$

where V_{OUT} is in volts and R is in kΩs.

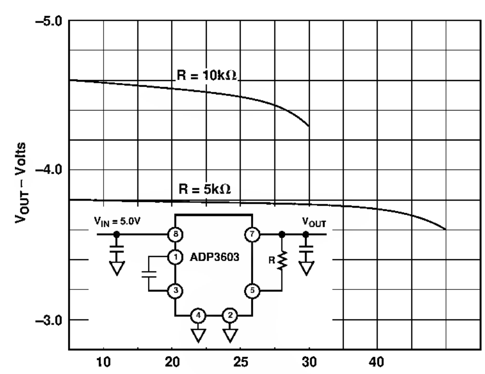


Figure 20. Maximum Regulated Output Voltage

POWER DISSIPATION

The power dissipation of the ADP3603 circuit must be limited such that the junction temperature of the device does not exceed the maximum junction temperature rating.

Power is dissipated in two components, power loss due to voltage drops in the switches, and power loss due to MOSFET drive current losses. Total power dissipation is calculated:

$$P \approx (V_{IN} - |V_{OUT}|)(I_{OUT}) + (V_{IN})(I_S)$$

where both V_{IN} and V_{OUT} are referred to ground pin of the ADP3603.

For example: Assuming the worst case conditions, $V_{IN} = 5.5$ V, $V_{OUT} = -2.85$ V, and $I_{OUT} = 50$ mA, calculated power dissipation is:

$$P \approx (5.5\ V - |-2.85\ V|)(0.05\ A) + (5.5\ V)(0.003\ A) = 149\ mW$$

This is far below the power dissipation capability of the ADP3603 package which is 660 mW.

LAYOUT AND GROUNDING TIPS

The ADP3603 switches turn on and off very fast. Good PC board layout practices will ensure the proper operation of the device. Important layout considerations include:

Use adequate ground and power traces or planes.

Keep components as close as possible to the device.

Use short trace lengths from the input and output capacitors to the input and output pins respectively.

Use single point ground for the device ground pins and the input and output capacitors.

Improper layouts will result in poor load regulation, especially with heavy loads.

APPLICATIONS

ADP3603 Evaluation Board Layout

The ADP3603 evaluation board is a general purpose circuit board. Its flexible design allows the user to optimize the circuit performance by external components selection and circuit configuration. The circuit board can be configured as a basic charge pump voltage inverter with one pump capacitor and two bypass capacitors or as a more complex circuit with input and output LC filters.

PC layout is designed for surface mount components and can be easily configured for through-hole components as well.

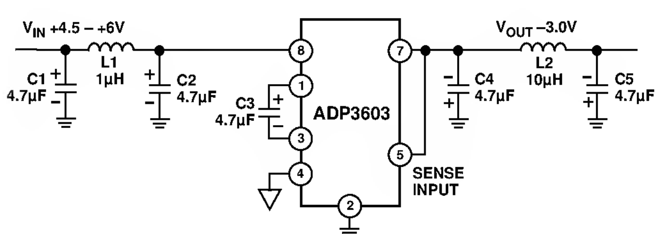


Figure 21. ADP3603 Evaluation Board Circuit Diagram

Table V. Recommended Components for Circuit in Figure 21

Component	Manufacturer/Type
C3	Sprague, 293D475X0035D2W
C1, C2, C4, C5	TOKIN, 1E475ZY5UC205F
L1	Coiltronics, CTX32CT-1R0
L2	Coiltronics, CTX32CT-100

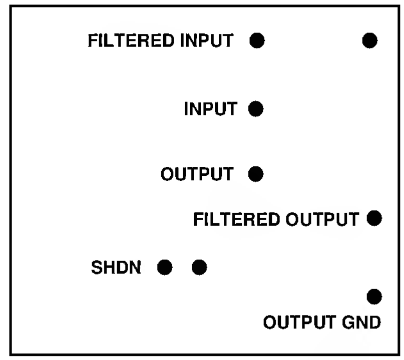


Figure 22. 8-Pin SOIC Layout, Wiring Connection

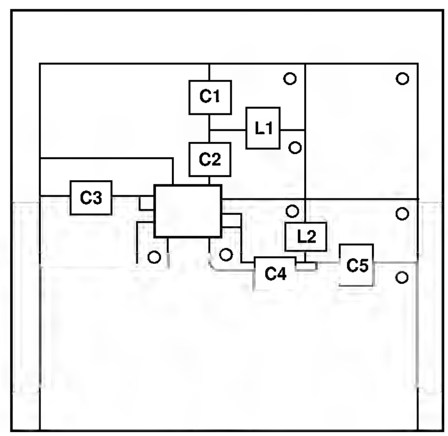


Figure 23. 8-Pin SOIC Layout, Component Placement Diagram (1× Scale)

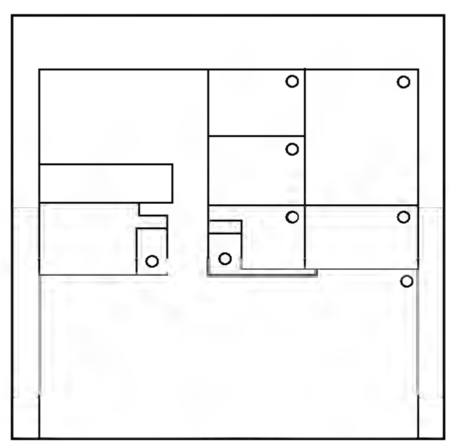
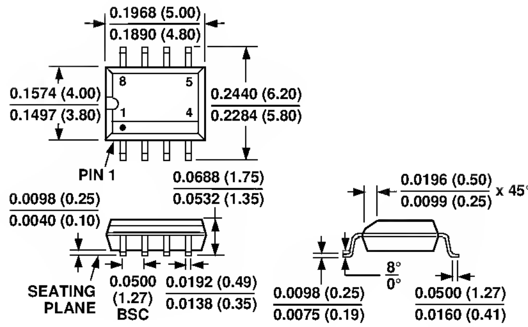


Figure 24. 8 Pin-SOIC Layout, Component Side (1× Layout)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Pin SOIC (SO-8)



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